ABSTRACT OF THE DISCLOSURE

A signal is transmitted in synchronization with a clock signal that repeats H and L levels indicating a preparation period and a transmission period, respectively. A transmitting circuit includes a transmitting capacitor, an input switch for setting a voltage in accordance with an input digital signal in the transmitting capacitor at preparation period, and a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor. A receiving circuit includes an inverter with a CMOS configuration, a receiving capacitor inserted between an input terminal and an output terminal of the inverter, an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set the voltage of the signal line to a predetermined voltage at preparation period, and a latch for supplying an output digital signal by performing logic amplification of the voltage of the output terminal of the inverter for each transmission period, and for holding the output for each preparation period.